forming a plurality of vertical type N channel transistors in a surface portion of the substrate before the forming the plurality of trenches, wherein

the surface portion is to be the first column, and

in the forming the plurality of trenches, each trench is disposed between two adjacent vertical type N channel transistors.

30. The method according to claim **28**, wherein

the forming the plurality of trenches includes measuring an impurity concentration of the substrate;

the forming the vertical type N channel transistor includes measuring a breakdown voltage of the vertical type N channel transistor,

the measuring the breakdown voltage includes heating the substrate in order to move an impurity ion from the second column into the oxide film when the breakdown voltage is smaller than a predetermined voltage, and

the heating the substrate is performed in such a manner that a product of the impurity concentration of the substrate and a width between two adjacent trenches is equalized to a product of the impurity concentration of the second conductive type semiconductor region and a width of the trench.

31. The method according to claim **30**, wherein

in the forming the second conductive type semiconductor region, the impurity concentration of the second conductive type semiconductor region is higher than the impurity concentration of the substrate.

32. The method according to claim **30**, wherein

in the forming the second conductive type semiconductor region, the product of the impurity concentration of the second conductive type semiconductor region and a thickness of the second conductive type semiconductor region is larger than the product of the impurity concentration of the substrate and the width between two adjacent trenches.

33. The method according to claim **26**, wherein

the substrate includes a dopant of phosphorous, arsenic or antimony.

34. The method according to claim **26**, wherein

the substrate has an impurity concentration in a range between 1×10^{15} cm^{-3} and 1×10^{18} cm^{-3}.

35. A method for manufacturing a semiconductor device comprising:

forming a plurality of trenches on a first side of a semiconductor substrate, wherein the substrate has a first conductive type;

forming a first conductive type semiconductor region on an inner wall of each trench by diffusing atoms in vapor phase or implanting ions into the inner wall of the trench, wherein an impurity concentration of the first conductive type semiconductor region is higher than an impurity concentration of the substrate, and wherein the substrate between the first conductive type semiconductor region in adjacent two trenches and the first conductive type semiconductor region in the adjacent two trenches provide a first column;

forming a second conductive type semiconductor film on the first conductive type semiconductor region in each trench so that the second conductive type semiconductor film in each trench provides a second column, wherein the first and second columns are alternately repeated along with a predetermined direction in parallel to the first side of the substrate;

thinning a second side of the substrate, the second side being opposite to the first side; and

increasing an impurity concentration of a thinned second side of the substrate so that a first conductive type layer is provided, wherein the impurity concentration of the first conductive type layer is higher than an impurity concentration of the first conductive type semiconductor region , wherein

a part of the substrate disposed on a periphery of the substrate provides a periphery layer, and

the first column provides a drift layer so that a vertical type first-conductive-type channel transistor is formed.

36. The method according to claim **35**, wherein

the first conductive type is a N conductive type, and the second conductive type is a P conductive type, and

the vertical type first-conductive-type channel transistor is a vertical type N channel transistor, the method further comprising:

forming a plurality of vertical type N channel transistors in a surface portion of the substrate before the forming the plurality of trenches, wherein

the surface portion is to be the first column, and

in the forming the plurality of trenches, each trench is disposed between two adjacent vertical type N channel transistors.

37. The method according to claim **35**, wherein

the first conductive type is a N conductive type, and the second conductive type is a P conductive type, and

the vertical type first-conductive-type channel transistor is a vertical type N channel transistor, the method further comprising:

forming the vertical type N channel transistor in a surface portion of the first column after the forming the second conductive type semiconductor film and before the thinning the second side.

38. A method for manufacturing a semiconductor device comprising:

forming a plurality of trenches on a first side of a semiconductor substrate, wherein the substrate has a first conductive type;

forming a first conductive type semiconductor region on an inner wall of each trench by an epitaxial growth method, wherein an impurity concentration of the first conductive type semiconductor region is higher than an impurity concentration of the substrate, and wherein the substrate between adjacent two trenches and the first conductive type semiconductor region in the adjacent two trenches provide a first column;

forming a second conductive type semiconductor film on the first conductive type semiconductor region in each trench so that the second conductive type semiconductor film in each trench provides a second column, wherein the first and second columns are alternately repeated along with a predetermined direction in parallel to the first side of the substrate;

thinning a second side of the substrate, the second side being opposite to the first side; and

increasing an impurity concentration of a thinned second side of the substrate so that a first conductive type layer is provided, wherein the impurity concentration of the first conductive type layer is higher than an impurity concentration of the first conductive type semiconductor region, wherein